WHAT IS CLAIMED IS:

1	1.	In a lo	ogic inverter; comprising an n-channel and a p-channel field-			
2	effect transistor, and	or, and a polysilicon gate extending over their respective channels, the				
3	improvement comprising:					
	-					
4		a)	a polysilicon conductor connecting drains of the two			
5	transistors.					
	2					
1	2.		ratus according to claim 1 in which the polysilicon conductor and			
2	the polysilicon gate a	are subs	tantially coplanar.			
1	3.	In an	integrated circuit which includes multiple layers of interconnect,			
2	the improvement cor					
_	in mprovement cor	pom	,			
3		a)	a layer of interconnect comprising local interconnect, and			
4	containing no non-lo	cal inte	rconnect.			
1	4.	In an	integrated circuit which includes multiple layers of interconnect,			
2 .	the improvement comprising:					
•		,	1100			
3		a)	different spacings between adjacent interconnect traces on one			
4	of the layers.					
1	5.	In a m	ethod of constructing a logic inverter which comprises an			
2			eld-effect transistor, the improvement comprising:			
_	in chainter and a p on	uiiiiQi II	old effect transistor, the improvement comprising.			
3		a)	etching			
4			i) a gate electrode and			
5			ii) a conductor connecting drains of the two transistors			
	from a simple larger	f 1	•			
6	from a single layer of	ı poıysı	ncon.			
1	6.	An in	egrated circuit, comprising:			
2		a)	a standard cell array comprising rows of cells having a row			
3	nitch: and					

4		b)	a MACRO, embedded within the standard cell array,	
5	comprising rows of cells having pitch substantially equal to the row pitch.			
1	7.	An ir	ntegrated circuit, comprising:	
2		a)	a standard cell array region, comprising rows of cells having a	
3	ROW PITCH;	,		
4		b)	a pair of power conductors extending across each row; and	
5		c)	a MACRO region, comprising rows of cells having a pitch	
6	equal to said row pitch.			
	-			
1	8.	An ir	ntegrated circuit, comprising:	
2		a)	cells of a standard cell array;	
3		b)	cells of a MACRO, which have different characteristics from	
4	those of the standard cell array and			
5		c)	parallel power conductors running adjacent all of said cells.	
1	9.	An in	itegrated circuit, comprising:	
2		a)	a MACRO embedded in a standard cell array, having	
3	substantially the same row pitch as that of the standard cell array;			
4		b)	parallel power busses which supply both the MACRO and the	
5	standard cell array;			
6		c)	a level of metallization which is free of local interconnect;	
7		d)	in said level of metallization, interconnect traces having non-	
8	uniform spacing; and	,	in said level of metamization, interconnect traces having non-	
O	umform spacing, and	•		
9		e)	CMOS inverters, utilized by the IC, in which drain-drain	
10	interconnect is constructed from polysilicon.			
1	10.	Appa	ratus according to claim 1 and further comprising a layer of	
2	interconnect traces which contains exclusively global interconnect.			

1	11.	Appar	atus according to claim 10 in which the layer of interconnect		
2	traces have a non-un	uniform spacing.			
1	12.	Appar	atus according to claim 1 and further comprising:		
2		b)	a standard cell array comprising rows of cells having a row		
3	pitch;				
4		c)	a MACRO, embedded within the standard cell array,		
5	comprising rows of	ells hav	ing pitch substantially equal to the row pitch.		
1	13.	A met	hod of constructing an integrated circuit, comprising the		
2	following steps:				
3		a)	running multiple computer simulations of a MACRO which is		
4			i) embedded in a standard cell array; and		
5			ii) constructed of transistors contained within the array;		
6		b)	changing dimensions of transistors in different simulations;		
7		c)	identifying transistor dimensions which provide superior timing		
8	performance; and				
9		d)	fabricating the embedded MACRO according to the identified		
10	dimensions of paragr	aph (c).			